

Substitute for form 1449A/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				Application Number	09/849799
				Filing Date	05/04/01
				First Named Inventor	G. Glenn Henry Thomas C. McDonald
				Group Art Unit	2183
				Examiner Name	Tonia Moenske
Sheet	1	of	2	Attorney Docket Number	CNTR.2052

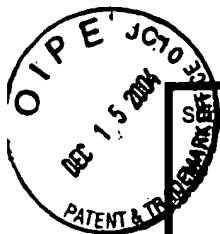
U.S. PATENT DOCUMENTS						
Examiner Initials	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ²			
TM	AA	5142634		Fite et al	08/25/1992	
TM	AB	5163140		Stiles et al	11/10/1992	
TM	AC	5353421		Emma et al	10/04/1994	
TM	AD	5355459		Matsuo et al	10/11/1994	
TM	AE	5404467		Saba et al	04/04/1995	
TM	AF	5530825		Black et al	06/25/1996	
TM	AG	5687360		Po-Hua Chang	11/11/1997	
TM	AH	5761723		Black et al	06/02/1998	
TM	AI	5812839		Hoyt et al	09/22/1998	
TM	AJ	5850543		Shiell et al	12/15/1998	
TM	AK	5867701		Brown et al	02/02/1999	
TM	AL	5948100		Hsu et al	09/07/1999	
TM	AM	5964868		Gochman et al	10/12/1999	
TM	AN	5974543		Hilgendorf et al	10/26/1999	
TM	AO	5978909		Oded Lempel	11/02/1999	
TM	AP	6044459		Bae et al	03/28/2000	
TM	AQ	6088793		Liu et al	07/11/2000	
TM	AR	6108773		Col et al	08/22/2000	
TM	AS	6151671		D'Sa et al	11/21/2000	
TM	AT	6314514		Thomas C. McDonald	11/6/2001	
TM	AU	6502185		Keller et al	12/31/2002	
TM	AV	6647467		Eric M. Dowling	11/11/2003	

Examiner Signature	<i>Tonia Moenske</i>	Date Considered	<i>July 8, 2006</i>
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OTHER PRIOR ART-NON PATENT LITERATURE DOCUMENTS			
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TM	BA	SAKAMOTO ET AL; <u>Microarchitecture Support for Reducing Branch Penalty in a Superscaler Processor</u> ; pp. 208-216; IEEE 1996; Mitsubishi Electric Corp., System LSI Laboratory, 4-1 Mizuhara, Itami, Hyogo 664, Japan.	
TM	BB	YEH ET AL; <u>ALTERNATIVE IMPLEMENTATION OF TWO-LEVEL ADAPTIVE BRANCH PREDICTION</u> ; 19 TH Annual International Symposium on Computer Architecture, pp. 124-134, May 19-21, 1992, Gold Coast, Australia.	
TM	BC	CHANG ET AL; <u>ALTERNATIVE IMPLEMENTATIONS OF HYBRID BRANCH PREDICTORS</u> ; Proceedings of MICRO-28, 1995, IEEE, pp. 252-257.	
TM	BD	MC FARLING, SCOTT; <u>WRL TECHNICAL NOTE TN-36, "Combining Branch Predictors</u> , June 1993, Western Research Laboratory, 250 University Ave., Palo Alto, CA 94301, pp. 1-25.	
TM	BE	IEEE 100; <u>THE AUTHORITATIVE DICTIONARY OF IEEE STANDARDS TERMS</u> ; Seventh Edition, IEEE, Standards Information Network, IEEE Press, 2000.	
TM	BF	BRAY ET AL; <u>STRATEGIES FOR BRANCH TARGET BUFFERS</u> ; Technical Report No. CSL-TR-91-480, June 1991, pp 1-21.	

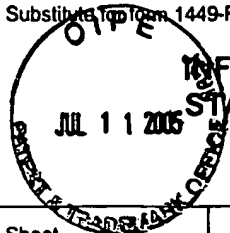
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Substitute Form 1449-PTO		Complete if Known	
 INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)		Application Number	09/849799
		Filing Date	5/4/2001
		First Named Inventor	G. Glenn Henry
		Art Unit	2183
		Examiner Name	Tonia Meonske
		Attorney Docket Number	CNTR.2052
Sheet	1	of	2

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
TM		5706491	01-06-1998	Steven C. McMahan	
TM		5313634	05-17-1994	James Eickemeyer	
TM		5961629	10-05-1999	Nguyen et al	
TM		5832289	11-03-1998	Shaw et al	
TM		5828901	10-27-1998	O'Toole et al	
TM		5864707	01-26-1999	Tran et al	
TM		6035391	03-07-2000	David L. Isaman	
TM		6081884	06-27-2000	Paul K. Miller	
TM		6250821	06-26-2001	Greg Schwendinger	
TM		5805877	09-08-1998	Black et al	
TM		6233676	05-15-2001	Henry et al	
TM		5623615	04-22-1997	Salem et al	
TM		6175897	01-16-2001	Ryan et al	
TM		5734881	03-31-1998	White et al	
TM		6260138	07-10-2001	Jeremy G. Harris	
TM		6823444	11-23-2004	Henry et al	
TM		6256727	07-03-2001	Robert Greg McDonald	
TM		5931944	08-03-1999	Ginosar et al	
TM		5881260	03-09-1999	Raje et al	
TM		4860197	08-22-1989	Langendorf et al	
TM		5513330	04-30-1996	David R. Stiles	
TM		6457120	09-24-2002	Balaram Sinharoy	
TM		5634103	05-27-1997	Dietz et al	
TM		5604877	02-18-1997	Hoyt et al	
TM		6134654	10-17-2000	Patel et al	

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**INFORMATION DISCLOSURE
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Sheet

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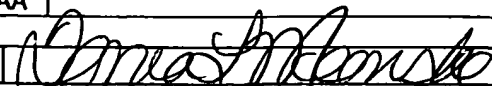
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		Number-Kind Code² (if known)			
TM		5687349	11-11-1997	Ralph C. McGarity	
TM		6279105	08-21-2001	Konigsburg et al	
TM		5881265	03-09-1999	McFarland et al	
TM		5968169	10-19-1999	James K. Pickett	
TM		6085311	07-04-2000	Narayan et al	
TM		6308259	10-23-2001	David B. Witt	
TM		5623614	04-22-1997	Van Dyke et al	
TM		5768576	06-16-1998	Hoyt et al	
TM		6170054	01-02-2001	Mitchell Alexander Poplingher	
TM		6279106	08-21-2001	James S. Roberts	
TM		5721855	02-24-1998	Hinton et al	
TM		6185676	02-06-2001	Poplingher et al.	
TM		5394530	02-28-1995	Mayumi Kitta	
TM		20040030866	02-12-2004	Thomas C. McDonald	
TM		20050044343	02-24-2005	Henry et al.	
TM		20040139281	07-15-2004	Thomas C. McDonald	
TM		20040139301	07-15-2004	Thomas C. McDonald	
TM		20040143727	07-22-2004	Thomas C. McDonald	
TM		20040143709	07-22-2004	Thomas C. McDonald	
TM		20040139292	07-15-2004	Thomas C. McDonald	
TM		20050076193	04-07-2005	Henry et al.	

NON PATENT LITERATURE DOCUMENTS

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TM	AA	IEEE 100, The Authoritative Dictionary of IEEE Standard Terms, Seventh Edition. The Institute of Electrical Engineering, Inc. New York: Standards Information Network IEEE Press Page 135, 2000.	

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July 8, 2006

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	BA	SAKAMOTO ET AL; <u>Microarchitecture Support for Reducing Branch Penalty in a Superscaler Processor</u> ; pp. 208-216; IEEE 1996; Mitsubishi Electric Corp., System LSI Laboratory, 4-1 Mizuhara, Itami, Hyogo 664, Japan.	
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	BD	MC FARLING, SCOTT; <u>WRL TECHNICAL NOTE TN-36, "Combining Branch Predictors</u> , June 1993, Western Research Laboratory, 250 University Ave., Palo Alto, CA 94301	
	BE	IEEE 100; <u>THE AUTHORITATIVE DICTIONARY OF IEEE STANDARDS TERMS</u> ; Seventh Edition, IEEE, Standards Information Network, IEEE Press,	
	BF	BRAY ET AL; <u>STRATEGIES FOR BRANCH TARGET BUFFERS</u> ; Technical Report No. CSL-TR-91-480, June 1991.	

Examiner Signature	<i>Tonia L. Moenske</i>	Date Considered	<i>July 8, 2006</i>
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TM	X	5752069	05-12-1998	Roberts et al.	

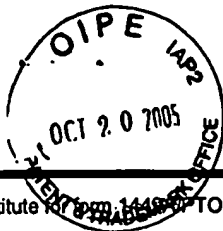
FOREIGN PATENT DOCUMENTS						
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TM	X	20050198481	09-08-2005	Henry et al.	
TM		20050198479	09-08-2005	Bean et al.	

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TM		6101595	08-08-2000	Pickett et al.	
TM		6157988	12-05-2000	Eric M. Dowling	
TM		6968444	11-22-2005	Kroesche et al.	
TM		6725357	04-20-2004	Jean Philippe Cousin	
TM		6041405	03-21-2000	Thomas S. Green	
TM		6754808	06-22-2004	Roth et al.	
TM		6374350	04-16-2002	D'Sa et al	
TM		5434985	07-18-1995	Emma et al	
TM		5553246	09-03-1996	Hiromi Suzuki	
TM		6122729	09-19-2000	Thang M. Tran	
TM		6748441	06-08-2004	David James Gemmell	
TM		6321321	11-20-2001	Mark W. Johnson	

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TM		Online Computing Dictionary. http://instantweb.com/d/dictionary/foldoc.cgi?query=btb 05/05/1995. Branch Target Buffer	
TM		The D Latch, Play-Hookey Web Page, Oct 10, 1999.	
TM		Patterson et al. "Computer Organization & Design: The Hardware/Software Interface." Morgan Kaufmann Publishers, Inc. San Francisco, CA. 1998 Page 469	
TM		Jimenez et al. "The Impact of Delay on the Design of Branch Predictors." 2000, PP1-ID.	
TM		EBERLY et al. "The Correlation Branch Target Address Cache" May 1996, IBM TDB, VOL 30-	
TM		Patterson et al. "Computer Organization & Design: The Hardware/Software Interface." Morgan Kaufmann Publishers, Inc. San Francisco, CA. 1998 Page 453-455	

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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				<i>Complete if Known</i>	
				Application Number	09/849799
				Filing Date	05/04/01
				First Named Inventor	G. Glenn Henry Thomas C. McDonald
				Group Art Unit	2183
				Examiner Name	Tonla Moenske
				Attorney Docket Number	CNTR.2052
Sheet	1	of	2		

U.S. PATENT DOCUMENTS						
Examiner Initials	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ²			
	AA	5142634		Fite et al	08/23/1992	
	AB	5163140		Stiles et al	11/10/1992	
	AC	5353421		Emma et al	10/04/1994	
	AD	5355459		Matsuo et al	10/11/1994	
	AE	5404467		Saba et al	04/04/1995	
	AF	5530825		Black et al	06/25/1996	
	AG	5687360		Po-Hua Chang	11/11/1997	
	AH	5761723		Black et al	06/02/1998	
	AI	5812839		Hoyt et al	09/22/1998	
	AJ	5850543		Shen et al	12/15/1998	
	AK	5867701		Brown et al	02/02/1999	
	AL	5948100		Hsu et al	09/07/1999	
	AM	5964868		Gochman et al	10/12/1999	
	AN	5974543		Hilgendorf et al	10/26/1999	
	AO	5978909		Oded Lempel	11/02/1999	
	AP	6044459		Bae et al	03/28/2000	
	AQ	6088793		Liu et al	07/11/2000	
	AR	6109773		Col et al	08/22/2000	
	AS	6151671		D'Sa et al	11/21/2000	
	AT	6314514		Thomas C. McDonald	11/6/2001	
	AU	6502185		Keller et al	12/31/2002	
	AV	6647467		Eric M. Dowling	11/11/2003	

Examiner Signature	<i>Ima L. Mendez</i>	Date Considered	<i>July 8, 2006</i>
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¹Priority claim designation number. ²See attached Kinds of U.S. Patent Documents. ³Enter Office that issued the document, by the two-letter code (WIPO Standard ST). ⁴For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 If possible. ⁶Applicant is to place a check mark here if English language Translation is attached.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Application Number	09/849799
		Filing Date	05/04/01
		First Named Inventor	G. Glenn Henry Thomas C. McDonald
		Group Art Unit	2183
		Examiner Name	Tonia Moenske
Sheet	2	of	2
		Attorney Docket Number	CNTR.2052

OTHER PRIOR ART-NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	BA	SAKAMOTO ET AL; <u>Microarchitecture Support for Reducing Branch Penalty in a Superscaler Processor</u> ; pp. 208-216; IEEE 1996; Mitsubishi Electric Corp., System LSI Laboratory, 4-1 Mizuhara, Itami, Hyogo 664, Japan.	
	BB	YEH ET AL; <u>ALTERNATIVE IMPLEMENTATION OF TWO-LEVEL ADAPTIVE BRANCH PREDICTION</u> ; 19 TH Annual International Symposium on Computer Architecture, pp. 124-134, May 19-21, 1992, Gold Coast, Australia.	
	BC	CHANG ET AL; <u>ALTERNATIVE IMPLEMENTATIONS OF HYBRID BRANCH PREDICTORS</u> ; Proceedings of MICRO-28, 1995, IEEE.	
	BD	MC FARLING, SCOTT; <u>WRL TECHNICAL NOTE TN-36, "Combining Branch Predictors</u> , June 1993, Western Research Laboratory, 250 University Ave., Palo Alto, CA 94301	
	BE	IEEE 100; <u>THE AUTHORITATIVE DICTIONARY OF IEEE STANDARDS TERMS</u> ; Seventh Edition, IEEE, Standards Information Network, IEEE Press,	
	BF	BRAY ET AL; <u>STRATEGIES FOR BRANCH TARGET BUFFERS</u> ; Technical Report No. CSL-TR-91-480, June 1991.	

Examiner Signature	<i>Tonia Moenske</i>	Date Considered	July 8, 2006
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